Amendments to the Specification:

Please replace the paragraph beginning on page 5, line 17 with the following amended paragraph:

Utilizing photolithography and dry etch processes, a series of contact openings are then formed at predetermined locations to form a bottom metal electrode 20. These contact openings will provide a contact path between predetermined areas of the semiconductor substrate 10 and the lower electrode of the capacitor. Next, a metal portion [[30]] 20 is deposited on the substrate 10, and a silicon nitride (SiN) portion 22 is sputtered on the metal portion [[30]] 20 to decrease leakage. Alternatively, other insulating film, such as undoped silicate glass (USG), borophosphosilicate glass (BPSG), or SiON, can be formed or deposited, including those described in U.S. Pat. No. 6,287,910 to Lee, et al. on Sep. 11, 2001. This insulating layer is then planarized, typically using a chemical mechanical polishing (CMP) process, to form an interlayer insulating film.

Please replace the paragraph beginning on page 7, line 8 with the following amended paragraph:

FIG. 2 shows an exemplary process for forming the capacitor of FIG. 1. First, the substrate 10 is prepared (step 52). Next, a bottom layer electrode is deposited (step 54). The silicon nitride 22 is then deposited (step 56), and followed by the deposition of the amorphous silicon 24 (step 58). Multiple sandwiched layers with alternating layer(s) of SiN 22 and Si 24 portions can be formed on the substrate 10. Finally, the metal 30 is deposited (step 60).

Please replace the lines beginning on page 8, line 3 to line 9 with the following amended lines:

2. Start sputtering Silicon with nitrogen gas to form a low leakage layer of SiN ~~(4A)~~ (202)

3. Remove nitrogen gas flow to deposit pure silicon ~~(40A)~~ (204)

4. Add nitrogen gas again to cap the layer off with SiN (which is insulating ~~40 A~~ 206)

Please replace the paragraph beginning on page 10, line 14 with the following amended paragraph:

Turning now to the short-range wireless transceiver core 330, the short-range wireless transceiver core 330 contains a radio frequency (RF) modem core 332 that communicates with a

link controller core 334. The processor core 350 controls the link controller core 334. In one embodiment, the RF modem core 332 has a direct-conversion radio architecture with integrated VCO and frequency synthesizer. The RF-unit 332 includes an RF receiver connected to an analog-digital converter (ADC), which in turn is connected to a modem [[316]] performing digital modulation, channel filtering, AFC, symbol timing recovery, and bit slicing operations. For transmission, the modem is connected to a digital to analog converter (DAC) that in turn drives an RF transmitter.